

JEDEC STANDARD

Definition of the SSTU32864 1.8-V Configurable Registered Buffer for DDR2 RDIMM Applications

JESD82-7A.01

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JEDEC SOLID STATE TECHNOLOGY ASSOCIATION



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DEFINITION OF THE SSTU32864 1.8-V CONFIGURABLE REGISTERED BUFFER FOR DDR2 RDIMM APPLICATIONS

(From JEDEC Board Ballot JCB-04-78, formulated under the cognizance of the JC-40 Committee on Digital Logic.)

1 Scope

This standard defines standard specifications of DC interface parameters, switching parameters, and test loading for definition of the SSTU32864 configurable registered buffer for DDR2 RDIMM applications.

The purpose is to provide a standard for the SSTU32864 (see Note) logic device, for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use.

NOTE The designation SSTU32864 refers to the part designation of a series of commercial logic parts common in the industry. This number is normally preceded by a series of manufacturer specific characters to make up a complete part designation.

2 Device Standard

2.1 Description

This 25-bit 1:1 or 14-bit 1:2 configurable registered buffer is designed for 1.7-V to 1.9-V V_{DD} operation.

All clock and data inputs are compatible with the JEDEC standard for SSTL_18. The control inputs are LVCMOS. All outputs are 1.8-V CMOS drivers that have been optimized to drive the DDR2 DIMM load.

The SSTU32864 operates from a differential clock (CK and \overline{CK}). Data are registered at the crossing of CK going high, and \overline{CK} going low.

The C0 input controls the pinout configuration of the 1:2 pinout from A configuration (when low) to B configuration (when high). The C1 input controls the pinout configuration from 25-bit 1:1 (when low) to 14-bit 1:2 (when high).

The device supports low-power standby operation. When the reset input (\overline{RESET}) is low, the differential input receivers are disabled, and undriven (floating) data, clock and reference voltage (V_{REF}) inputs are allowed. In addition, when \overline{RESET} is low all registers are reset, and all outputs are forced low. The LVCMOS \overline{RESET} and Cn inputs must always be held at a valid logic high or low level.

To ensure defined outputs from the register before a stable clock has been supplied, \overline{RESET} must be held in the low state during power up.

2 Device Standard (cont'd)

2.1 Description (cont'd)

In the DDR2 RDIMM application, $\overline{\text{RESET}}$ is specified to be completely asynchronous with respect to CK and $\overline{\text{CK}}$. Therefore, no timing relationship can be guaranteed between the two. When entering reset, the register will be cleared and the outputs will be driven low quickly, relative to the time to disable the differential input receivers. However, when coming out of reset, the register will become active quickly, relative to the time to enable the differential input receivers. As long as the data inputs are low, and the clock is stable during the time from the low-to-high transition of $\overline{\text{RESET}}$ until the input receivers are fully enabled, the design of the SSTU32864 must ensure that the outputs will remain low, thus ensuring no glitches on the output.

The device monitors both $\overline{\text{DCS}}$ and $\overline{\text{CSR}}$ inputs and will gate the Qn outputs from changing states when both $\overline{\text{DCS}}$ and $\overline{\text{CSR}}$ inputs are high. If either $\overline{\text{DCS}}$ or $\overline{\text{CSR}}$ input is low, the Qn outputs will function normally. The $\overline{\text{RESET}}$ input has priority over the $\overline{\text{DCS}}$ and $\overline{\text{CSR}}$ control and will force the outputs low. If the $\overline{\text{DCS}}$ -control functionality is not desired, then the $\overline{\text{CSR}}$ input can be hardwired to ground, in which case, the setup-time requirement for $\overline{\text{DCS}}$ would be the same as for the other D data inputs.

Package options include 96-ball Low Profile Fine Pitch BGA (LFBGA) (16 x 6 Array, 13.50 x 5.50 mm body size, 0.80 mm pitch, MO-205, Variation CC).

2.2 96-ball LFBGA (MO-205CC)

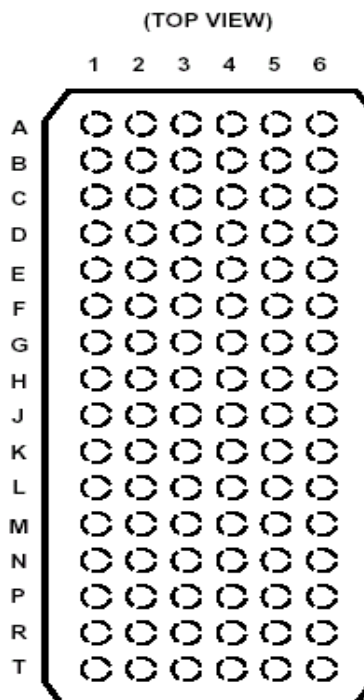


Figure 1 — Pinout Configuration

2.3 Pinout Top View for 96-ball LFBGA

NC denotes a no-connect (ball present but not connected to the die). DNU denotes a do-not-use pin (ball connected to the die but should be left open-circuit).

A	DCKE	NC	V _{REF}	V _{DD}	QCKE	DNU
B	D2	D15	GND	GND	Q2	Q15
C	D3	D16	V _{DD}	V _{DD}	Q3	Q16
D	DODT	NC	GND	GND	QODT	DNU
E	D5	D17	V _{DD}	V _{DD}	Q5	Q17
F	D6	D18	GND	GND	Q6	Q18
G	NC	$\overline{\text{RESET}}$	V _{DD}	V _{DD}	C1	C0
H	CK	$\overline{\text{DCS}}$	GND	GND	$\overline{\text{QCS}}$	DNU
J	$\overline{\text{CK}}$	$\overline{\text{CSR}}$	V _{DD}	V _{DD}	ZOH	ZOL
K	D8	D19	GND	GND	Q8	Q19
L	D9	D20	V _{DD}	V _{DD}	Q9	Q20
M	D10	D21	GND	GND	Q10	Q21
N	D11	D22	V _{DD}	V _{DD}	Q11	Q22
P	D12	D23	GND	GND	Q12	Q23
R	D13	D24	V _{DD}	V _{DD}	Q13	Q24
T	D14	D25	V _{REF}	V _{DD}	Q14	Q25
	1	2	3	4	5	6

Figure 2 — 1:1 Register (C0=0, C1=0)

A	DCKE	NC	V _{REF}	V _{DD}	QCKEA	QCKEB
B	D2	DNU	GND	GND	Q2A	Q2B
C	D3	DNU	V _{DD}	V _{DD}	Q3A	Q3B
D	DODT	NC	GND	GND	QODTA	QODTB
E	D5	DNU	V _{DD}	V _{DD}	Q5A	Q5B
F	D6	DNU	GND	GND	Q6A	Q6B
G	NC	$\overline{\text{RESET}}$	V _{DD}	V _{DD}	C1	C0
H	CK	$\overline{\text{DCS}}$	GND	GND	$\overline{\text{QCSA}}$	$\overline{\text{QCSB}}$
J	$\overline{\text{CK}}$	$\overline{\text{CSR}}$	V _{DD}	V _{DD}	ZOH	ZOL
K	D8	DNU	GND	GND	Q8A	Q8B
L	D9	DNU	V _{DD}	V _{DD}	Q9A	Q9B
M	D10	DNU	GND	GND	Q10A	Q10B
N	D11	DNU	V _{DD}	V _{DD}	Q11A	Q11B
P	D12	DNU	GND	GND	Q12A	Q12B
R	D13	DNU	V _{DD}	V _{DD}	Q13A	Q13B
T	D14	DNU	V _{REF}	V _{DD}	Q14A	Q14B
	1	2	3	4	5	6

Figure 3 — 1:2 Register A (C0=0, C1=1)

2.3 Pinout Top View for 96-ball LFBGA (cont'd)

A	D1	NC	V _{REF}	V _{DD}	Q1A	Q1B
B	D2	DNU	GND	GND	Q2A	Q2B
C	D3	DNU	V _{DD}	V _{DD}	Q3A	Q3B
D	D4	NC	GND	GND	Q4A	Q4B
E	D5	DNU	V _{DD}	V _{DD}	Q5A	Q5B
F	D6	DNU	GND	GND	Q6A	Q6B
G	NC	$\overline{\text{RESET}}$	V _{DD}	V _{DD}	C1	C0
H	CK	$\overline{\text{DCS}}$	GND	GND	$\overline{\text{QCSA}}$	$\overline{\text{QCSB}}$
J	$\overline{\text{CK}}$	$\overline{\text{CSR}}$	V _{DD}	V _{DD}	ZOH	ZOL
K	D8	DNU	GND	GND	Q8A	Q8B
L	D9	DNU	V _{DD}	V _{DD}	Q9A	Q9B
M	D10	DNU	GND	GND	Q10A	Q10B
N	DODT	DNU	V _{DD}	V _{DD}	QODTA	QODTB
P	D12	DNU	GND	GND	Q12A	Q12B
R	D13	DNU	V _{DD}	V _{DD}	Q13A	Q13B
T	DCKE	DNU	V _{REF}	V _{DD}	QCKEA	QCKEB
	1	2	3	4	5	6

Figure 4 — 1:2 Register B (C0=1, C1=1)

2 Device Standard (cont'd)

2.4 Terminal Functions

Table 1 — Terminal Functions

Terminal Name	Description	Electrical Characteristics
GND	Ground	Ground input
V _{DD}	Power supply voltage	1.8-V nominal
V _{REF}	Input reference voltage	0.9-V nominal
Z _{OH}	Reserved for future use	Input
Z _{OL}	Reserved for future use	Input
CK	Positive main clock input	Differential input
$\overline{\text{CK}}$	Negative main clock input	Differential input
C0, C1	Configuration control inputs	LVC MOS inputs
$\overline{\text{RESET}}$	Asynchronous reset input – resets registers and disables V _{REF} data and clock differential-input receivers	LVC MOS input
$\overline{\text{CSR}}$, $\overline{\text{DCS}}$	Chip select inputs – disables data outputs switching when both inputs are high (see Note)	SSTL_18 input
D1–D25	Data input – clocked in on the crossing of the rising edge of CK and the falling edge of $\overline{\text{CK}}$	SSTL_18 input
DODT	The outputs of this register bit will not be suspended by the $\overline{\text{DCS}}$ and $\overline{\text{CSR}}$ control.	SSTL_18 input
DCKE	The outputs of this register bit will not be suspended by the $\overline{\text{DCS}}$ and $\overline{\text{CSR}}$ control.	SSTL_18 input
Q1–Q25	Data outputs that are suspended by the $\overline{\text{DCS}}$ and $\overline{\text{CSR}}$ control (see Note 2).	1.8-V CMOS
$\overline{\text{QCS}}$	Data output that will not be suspended by the $\overline{\text{DCS}}$ and $\overline{\text{CSR}}$ control.	1.8-V CMOS
QODT	Data output that will not be suspended by the $\overline{\text{DCS}}$ and $\overline{\text{CSR}}$ control.	1.8-V CMOS
QCKE	Data output that will not be suspended by the $\overline{\text{DCS}}$ and $\overline{\text{CSR}}$ control.	1.8-V CMOS
NC	No-connect. Ball present but no internal connection to the die.	
DNU	Do-not-use. Ball internally connected to the die which should be left open-circuit.	
<p>NOTE 1 Configurations: Data inputs = D2, D3, D5, D6, D8-D25 when C0 = 0 and C1 = 0. Data inputs = D2, D3, D5, D6, D8-D14 when C0 = 0 and C1 = 1. Data inputs = D1-D6, D8-D10, D12, D13 when C0 = 1 and C1 = 1.</p> <p>NOTE 2 Configurations: Data outputs = Q2, Q3, Q5, Q6, Q8-Q25 when C0 = 0 and C1 = 0. Data outputs = Q2, Q3, Q5, Q6, Q8-Q14 when C0 = 0 and C1 = 1. Data outputs = Q1-Q6, Q8-Q10, Q12, Q13 when C0 = 1 and C1 = 1.</p>		

2.5 Function Table

Inputs						Outputs		
$\overline{\text{RESET}}$	$\overline{\text{DCS}}$	$\overline{\text{CSR}}$	CK	$\overline{\text{CK}}$	Dn, DODT, DCKE	Qn	$\overline{\text{QCS}}$	QODT, QCKE
H	L	L	↑	↓	L	L	L	L
H	L	L	↑	↓	H	H	L	H
H	L	L	L or H	L or H	X	Q ₀	Q ₀	Q ₀
H	L	H	↑	↓	L	L	L	L
H	L	H	↑	↓	H	H	L	H
H	L	H	L or H	L or H	X	Q ₀	Q ₀	Q ₀
H	H	L	↑	↓	L	L	H	L
H	H	L	↑	↓	H	H	H	H
H	H	L	L or H	L or H	X	Q ₀	Q ₀	Q ₀
H	H	H	↑	↓	L	Q ₀	H	L
H	H	H	↑	↓	H	Q ₀	H	H
H	H	H	L or H	L or H	X	Q ₀	Q ₀	Q ₀
L	X or Floating	X or Floating	X or Floating	X or Floating	X or Floating	L	L	L

2 Device Standard (cont'd)
2.6 Logic Diagram

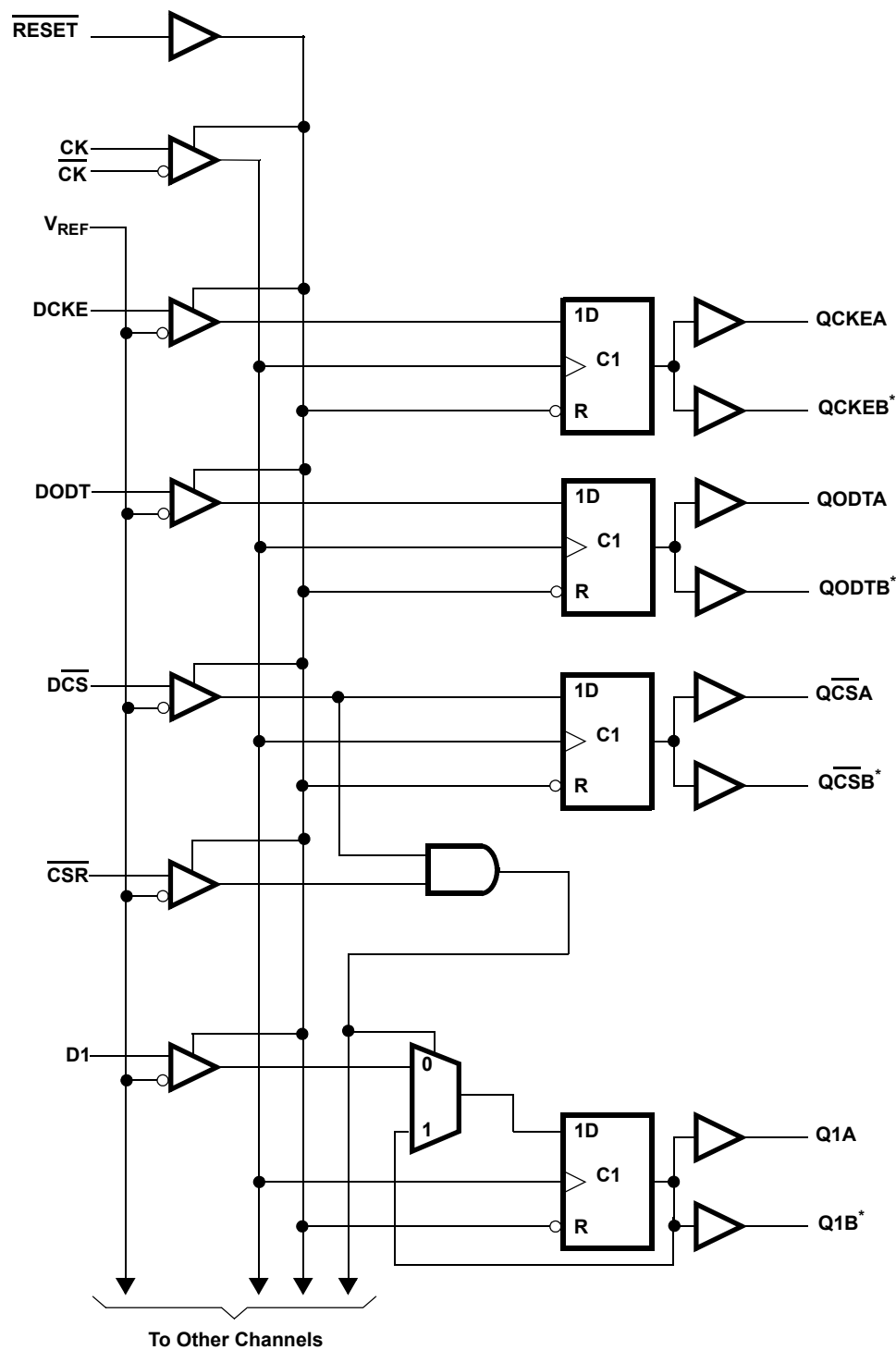


Figure 5 — Logic Diagram 1:2 Mode (Positive Logic)

2 Device Standard (cont'd)

2.7 Absolute Maximum Ratings

Table 3 — Absolute Maximum Ratings over Operating Free-air Temperature Range (see Note 1)

Supply voltage range, V_{DD}	–0.5 V to 2.5 V
Input voltage range, V_I (See Notes 2 and 3)	–0.5 V to 2.5 V
Output voltage range, V_O (See Notes 2 and 3)	–0.5 V to $V_{DD} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{DD}$)	± 50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{DD}$)	± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{DD})	± 50 mA
Continuous current through each V_{DD} or GND	± 100 mA
Storage temperature range, T_{STG}	–65 °C to 150 °C

NOTE 1 Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 2 The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

NOTE 3 This value is limited to 2.5 V maximum.

2.8 Recommended Operating Conditions

Table 4 — Recommended Operating Conditions (see NOTE 1)

			Min	Nom	Max	Unit
V_{DD}	Supply voltage		1.7		1.9	V
V_{REF}	Reference voltage		$0.49 * V_{DD}$	$0.5 * V_{DD}$	$0.51 * V_{DD}$	V
V_{TT}	Termination voltage		$V_{REF} - 40$ mV	V_{REF}	$V_{REF} + 40$ mV	V
V_I	Input voltage		0		V_{DD}	V
V_{IH}	AC high-level input voltage	Data inputs, \overline{CSR}	$V_{REF} + 250$ mV			V
V_{IL}	AC low-level input voltage	Data inputs, \overline{CSR}			$V_{REF} - 250$ mV	V
V_{IH}	DC high-level input voltage	Data inputs, \overline{CSR}	$V_{REF} + 125$ mV			V
V_{IL}	DC low-level input voltage	Data inputs, \overline{CSR}			$V_{REF} - 125$ mV	V
V_{IH}	High-level input voltage	\overline{RESET} , Cn	$0.65 * V_{DD}$			V
V_{IL}	Low-level input voltage	\overline{RESET} , Cn			$0.35 * V_{DD}$	V
V_{ICR}	Common-mode input range	CK, \overline{CK}	0.675		1.125	V
V_{ID}	Differential input voltage	CK, \overline{CK}	600			mV
I_{OH}	High-level output current				–8	mA
I_{OL}	Low-level output current				8	
T_A	Operating free-air temperature		0		70	°C

NOTE 1 The \overline{RESET} and Cn inputs of the device must be held at valid logic levels (not floating) to ensure proper device operation. The differential inputs must not be floating, unless \overline{RESET} is low.

2.9 DC Specifications

Parameter		Test conditions		V _{DD}	Min	Typ	Max	Unit
V _{OH}		I _{OH} = −6 mA		1.7 V	1.2			V
V _{OL}		I _{OL} = 6 mA		1.7 V			0.5	V
I _I	All inputs	V _I = V _{DD} or GND		1.9 V	−5		+5	μA
I _{DD}	Static standby	$\overline{\text{RESET}} = \text{GND}$	I _O = 0	1.9 V			100	μA
	Static operating	$\overline{\text{RESET}} = \text{V}_{\text{DD}}$, V _I = V _{IH(AC)} or V _{IL(AC)}					40	mA
I _{DDD}	Dynamic operating – clock only	$\overline{\text{RESET}} = \text{V}_{\text{DD}}$, V _I = V _{IH(AC)} or V _{IL(AC)} , CK and $\overline{\text{CK}}$ switching 50% duty cycle	I _O = 0	1.8 V		†		μA/ clock MHz
	Dynamic operating – per each data input, 1:1 mode	$\overline{\text{RESET}} = \text{V}_{\text{DD}}$, V _I = V _{IH(AC)} or V _{IL(AC)} , CK and $\overline{\text{CK}}$ switching 50% duty cycle. One data input switching at half clock frequency, 50% duty cycle.				†		μA/ clock MHz/ data input
	Dynamic operating – per each data input, 1:2 mode	$\overline{\text{RESET}} = \text{V}_{\text{DD}}$, V _I = V _{IH(AC)} or V _{IL(AC)} , CK and $\overline{\text{CK}}$ switching 50% duty cycle. One data input switching at half clock frequency, 50% duty cycle.				†		
C _i	Data inputs, $\overline{\text{CSR}}$	V _I = V _{REF} ± 250 mV		1.8 V	2.5		3.5	pF
	CK and $\overline{\text{CK}}$	V _{ICR} = 0.9 V, V _{ID} = 600 mV			2		3	
	RESET	V _I = V _{DD} or GND			†		†	
NOTE † The vendor must supply this value for full device description.								

2 Device Standard (cont'd)

2.10 Timing requirements

Table 6 — Timing Requirements over Recommended Operating Free-air Temperature Range (see Figure 6)

Symbol	Parameter	Conditions	$V_{DD} = 1.8\text{ V} \pm 0.1\text{ V}$		Unit
			Min	Max	
f_{clock}	Clock frequency			270	MHz
t_w	Pulse duration, CK, $\overline{\text{CK}}$ high or low		1		ns
t_{act}^1	Differential inputs active time (see NOTE 2)			10	ns
t_{inact}^1	Differential inputs inactive time (see NOTE 3)			15	ns
t_{su}	Setup time	$\overline{\text{DCS}}$ before CK \uparrow , $\overline{\text{CK}}$ \downarrow , $\overline{\text{CSR}}$ high; $\overline{\text{CSR}}$ before CK \uparrow , $\overline{\text{CK}}$ \downarrow , $\overline{\text{DCS}}$ high	0.7		ns
t_{su}	Setup time	$\overline{\text{DCS}}$ before CK \uparrow , $\overline{\text{CK}}$ \downarrow , $\overline{\text{CSR}}$ low	0.5		ns
t_{su}	Setup time	ODT, CKE, and data before CK \uparrow , $\overline{\text{CK}}$ \downarrow	0.5		ns
t_h	Hold time	$\overline{\text{DCS}}$, ODT, CKE, and data after CK \uparrow , $\overline{\text{CK}}$ \downarrow	0.5		ns
NOTE 1 This parameter is not necessarily production tested.					
NOTE 2 Data and V_{REF} inputs must be low a minimum time of t_{act} max, after $\overline{\text{RESET}}$ is taken high					
NOTE 3 Data, V_{REF} and clock inputs must be held at valid levels (not floating) a minimum time of t_{inact} max, after $\overline{\text{RESET}}$ is taken low.					

2.11 AC Specifications

Table 7 — Switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 6)

Parameter	From (Input)	To (Output)	$V_{DD} = 1.8\text{ V} \pm 0.1\text{ V}$		Unit
			Min	Max	
f_{max}			270		MHz
t_{pdm}^1	CK and $\overline{\text{CK}}$	Q	1.41	2.15	ns
t_{pdmss} (Simultaneous switching) ^{1,2}	CK and $\overline{\text{CK}}$	Q		2.35	ns
t_{RPHL}	$\overline{\text{RESET}}$	Q		3	ns
NOTE 1 Includes 350 ps test-load transmission-line delay.					
NOTE 2 This parameter is not necessarily production tested.					

3

Output Buffer Characteristics

Table 8 — Output Edge Rates Over Recommended Operating Free-air Temperature Range
(See Figure 7)

Parameter	V _{DD} = 1.8 V ± 0.1 V		Unit
	Min	Max	
dV/dt_r	1	4	V/ns
dV/dt_f	1	4	V/ns
dV/dt_Δ ¹		1	V/ns
NOTE 1 Difference between dV/dt_r (rising edge rate) and dV/dt_f (falling edge rate).			

4 Test Circuits and Switching Waveforms

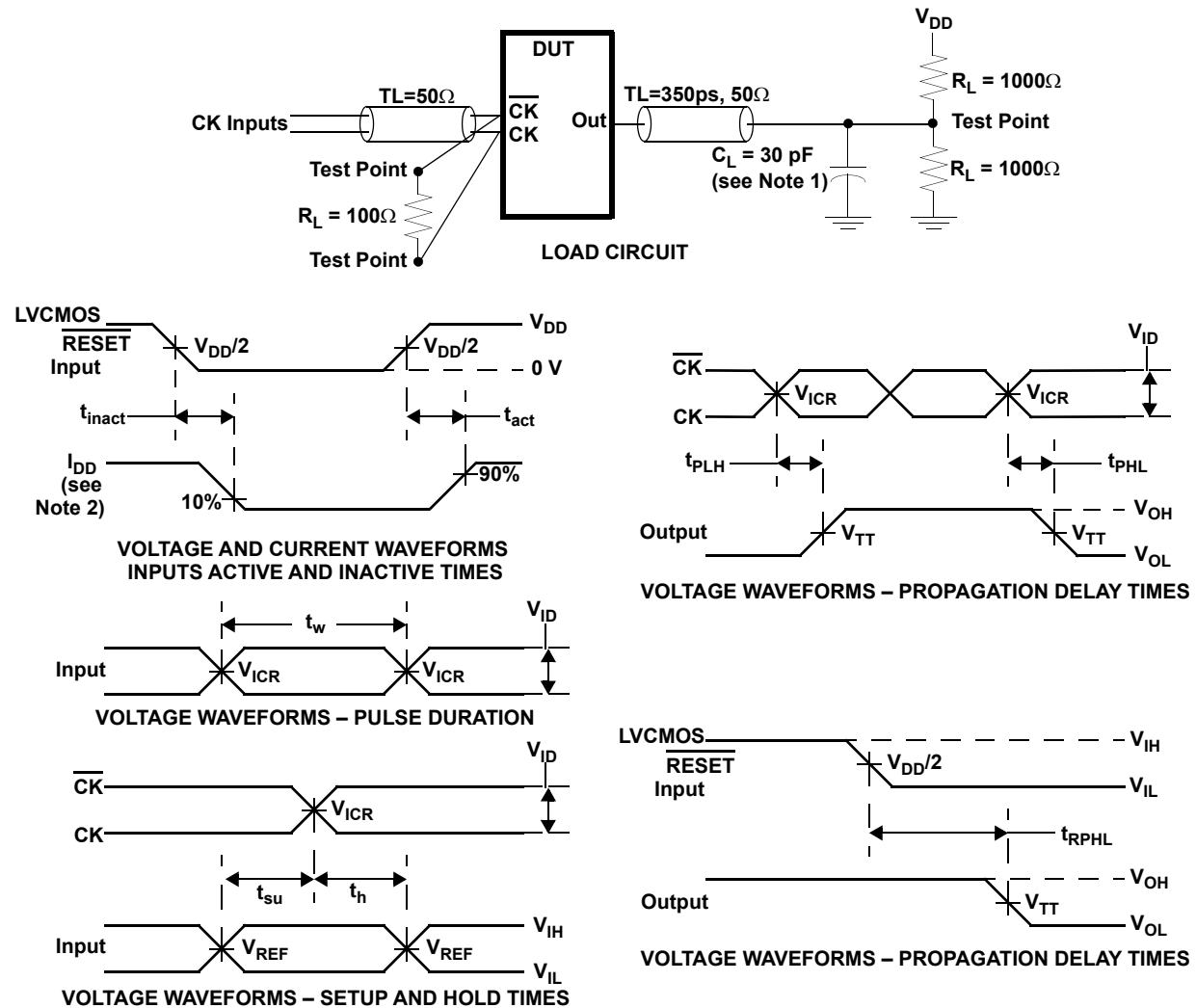


Figure 6 — Parameter Measurement Information ($V_{DD} = 1.8 \text{ V} \pm 0.1 \text{ V}$)

NOTE 1 C_L includes probe and jig capacitance.

NOTE 2 I_{DD} tested with clock and data inputs held at V_{DD} or GND, and $I_O = 0 \text{ mA}$.

NOTE 3 All input pulses are supplied by generators having the following characteristics: Pulse Repetition Rate $\leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, input slew rate = $1 \text{ V/ns} \pm 20\%$ (unless otherwise specified).

NOTE 4 The outputs are measured one at a time with one transition per measurement.

NOTE 5 $V_{REF} = V_{DD}/2$

NOTE 6 $V_{IH} = V_{REF} + 250 \text{ mV}$ (ac voltage levels) for differential inputs. $V_{IH} = V_{DD}$ for LVC MOS input.

NOTE 7 $V_{IL} = V_{REF} - 250 \text{ mV}$ (ac voltage levels) for differential inputs. $V_{IL} = \text{GND}$ for LVC MOS input.

NOTE 8 $V_{ID} = 600 \text{ mV}$

NOTE 9 t_{PLH} and t_{PHL} are the same as t_{pdm}

4 Test Circuits and Switching Waveforms (cont'd)

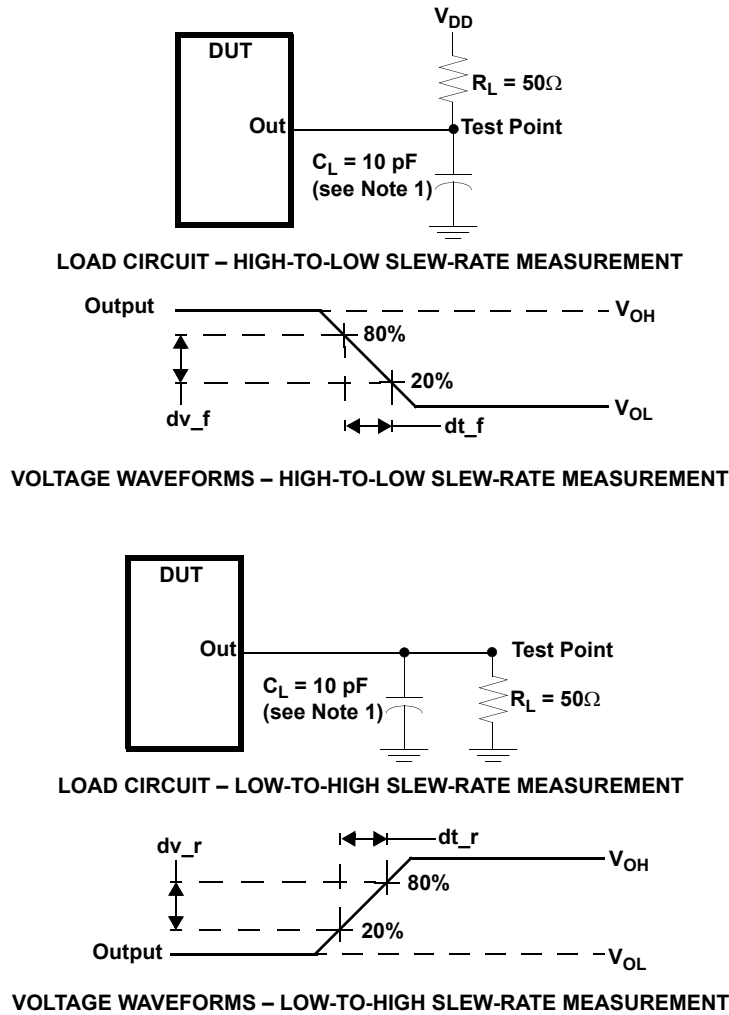


Figure 7 — Output Slew-Rate Measurement Information ($V_{DD} = 1.8\text{ V} \pm 0.1\text{ V}$)

NOTE 1 C_L includes probe and jig capacitance.

NOTE 2 All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\Omega$, input slew rate = $1\text{ V/ns} \pm 20\%$ (unless otherwise specified).

5 Reference to Other Applicable JEDEC Standards and Publications

- JEP95, *JEDEC Registered and Standard Outlines for Solid State and Related Products.*
- JEP104, *Reference Guide to Letter Symbols for Semiconductor Devices.*
- JESD8-7, *1.8V +/- 0.15V (Normal Range), and 1.2 - 1.95V (Wide Range) Power Supply Voltage and Interface for Non-terminated Digital Integrated Circuits.*
- JESD8-15, *Stub Series Terminated Logic for 1.8 V (SSTL_18).*
- JESD21-C, *Configuration for Solid State Memories.*

Annex A — (Informative) Differences between JESD82-7A and JESD82-4

This annex briefly describes most of the changes made to entries that appear in this standard, JESD82-7A, compared to its predecessor, JESD82-7 (November 2002). If the change to a concept involves any words added or deleted (excluding deletion of accidentally repeated words), it is included. Some punctuation changes are not included.

- Resolved TBD and provisional parameter values in Tables 4, 5, 6 and 7.
- Assigned and clarified DNU (do not use) pins to ballout and Terminal Functions (Table 1).
- Provided voltage and current conditions for Table 5.
- Editorial updates.

Annex A — (Informative) Differences between JESD82-7A and JESD82-4

Editorial changes as follows:

1. Terminology update: Table 1 - Changed “master” to “main” for description of CK and $\overline{\text{CK}}$
2. Updated JEDEC logos and Standard Improvement Form
3. All section headings, table titles, and figure titles changed to Initial Caps
4. Table layouts updated to JEDEC standard format

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